A 44 GHz Low Noise Block Downconvertor MMIC suitable for EHF satellite communication applications

A R Barnes, D C Bannister and M T Moore

Defence Evaluation Research Agency, St Andrews Road, Malvern, UK, WR14 3PS

ABSTRACT

A multifunction MMIC, containing the core components required for an EHF satellite communications receiver, operating over 43.5 to 45.5GHz, has been designed and tested. The circuit has been fabricated using a high yield, commercially available, 0.25µm PHEMT GaAs - InGaAs - AlGaAs foundry process at GEC Marconi Materials Technology Ltd. The multifunction MMIC integrates a low noise amplifier, downconvertor, local oscillator doubler and buffer amplifier onto a single chip occupying an area of 3.0 x 3.8mm^2. Successful performance was achieved for a first pass iteration, namely 4.3dB noise figure and 5 to 8dB conversion gain with a low local oscillator (LO) drive level of 0dBm.

1 Introduction

There is an increasing demand for more sophisticated military satellite communication systems, (a) to ensure secure communications in times of tension or war and (b) due to more demanding end user requirements, eg large numbers of computers exchanging digital information as part of Command, Control, Communications and Intelligence (C^{3}I) networks.

Exploitation of EHF frequency bands for next generation military satellite communications offers a number of advantages over UHF and SHF solutions including improved protection against jamming, low probability of intercept and minimal disruption to earth-space propagation in the presence of high altitude nuclear explosions[(1)]. Moving to EHF operating frequencies means that antenna size is reduced allowing compact phased arrays to be deployed on satellites. Phased array antennas offer the potential for beam nulling or the deployment of spot beams to provide further immunity from jamming.

MMICs are a key enabling technology for EHF phased arrays due to their small size, improved reliability, high repeatability and the potential for low cost. Multifunction MMICs, integrating several functions onto a single chip, are particularly attractive at mm-wave frequencies since they allow considerable size and weight reduction along with improved reliability from having fewer components. In addition, circuit performance is less compromised by interface parasitics of multiple tape bonds used to connect together many individual building block functions.

The level of integration that can be accommodated is a function of the manufacturing process yield, testing requirements and the accuracy of CAD design tools. A careful balance has to be made between the level of integration that is practical without compromising circuit yield. This paper addresses the design, fabrication and assessment of a high yield multifunction MMIC integrating the core elements required in an EHF receiver; low noise amplifier, downconvertor, local oscillator doubler and buffer amplifier.

2 Circuit design and measured performance

A high level of gain (> 100dB) is required in an EHF receiver to boost the low power signals at the receive antenna to an acceptable level. The majority of amplification is usually performed at IF, since gain blocks at these frequencies are relatively inexpensive. For our application, 25dB of RF gain was desired in order to minimise the noise contribution of following stages. A simplified schematic of the EHF receiver architecture is shown in figure 1, consisting of a front end low noise amplifier, low noise block downconvertor (LNB), bandpass filters and IF amplifiers. The aim of this work was to demonstrate a low cost, high yield, low noise block downconvertor (LNB) MMIC that could be used at the heart of an EHF satellite communications receiver. The design target was 6dB conversion gain and sub 5dB noise figure with the intention of using the chip in conjunction with a 20dB gain, 2.5dB noise figure, front end LNA to achieve an overall system noise figure of 3dB and 25dB RF conversion gain.

A commercially available 0.25µm PHEMT foundry process (H40) from GEC Marconi Materials Technology was used for this work (f_t=60GHz, NF_{min}=0.7dB at 12GHz). This process was chosen since it offers an accurate model database and high yield capability. In addition to using standard foundry models, non-linear physics based models[(2)] were used to analyse the performance of the local oscillator doubler-buffer amplifier.

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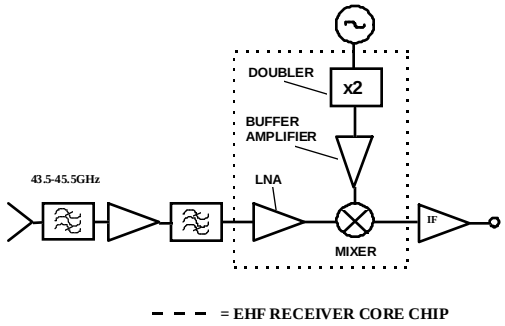

Figure 1 : EHF receiver architecture

All circuit design work was performed using Libra*. Electromagnetic simulation, using Sonnet EM**, was found to be essential in analysing the effects of unwanted coupling at these frequencies. To aid measurement diagnostics, individual receiver building block functions were also included on the MMIC wafer. The design and measured performance of these components is now described along with the measured response of the single chip low noise block downconvertor.

2.1 Low noise amplifier

The target specification for the low noise amplifier was 15dB gain, 3.5dB noise figure and >12dB port return loss. In order to satisfy the gain requirement a three stage design was chosen using 4x40µm gate width devices. This device size was used since it was found to simplify the matching network topology for minimum noise figure. Stages 1 and 2 were biased for low noise operation (Vds=2V at 10mA) and stage 3 for high gain (Vds=2V at 20mA). The first stage used series inductive feedback to help achieve a simultaneous noise-input match and to aid in-band stability. Out of band stability was achieved using resistive loading in the gate bias line.

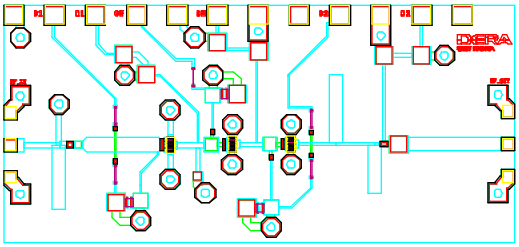

Figure 2 : Low noise amplifier layout

The chip layout is shown in figure 2 and occupies an area of 3.2 x 1.6mm^2. A comparison between measured and simulated performance is shown in figure 3, illustrating that over the 43.5 to 45.5GHz frequency range the measured noise figure was 3.6-3.8dB with an associated gain of 13dB. Input and output port return loss was typically better than 15dB. Measured results agree well with simulation, with the exception of gain which is 3 to 4 dB lower than predicted. This is believed to be due to a higher than expected output conductance, g_0, for this process run.

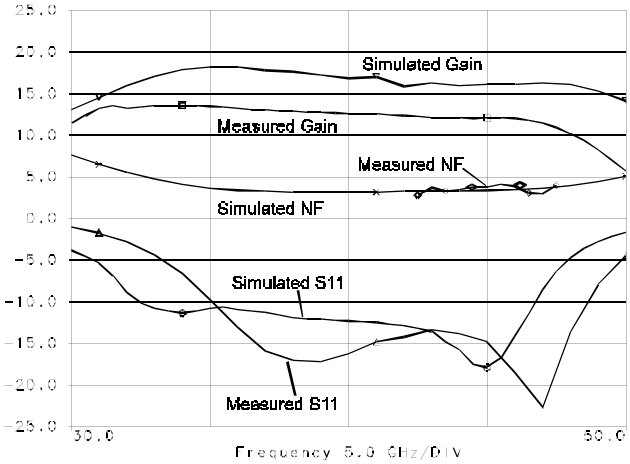

Figure 3 : Measured and modelled LNA performance

2.2 Mixer

A passive diode approach was chosen for the mixer design to allow both downconvert operation, as required for the receiver application described here, and also upconvert operation to allow the same component to be used in transmit uplink applications. In order to perform non-linear analysis, multi-bias S-parameter measurements were made over the 0.5 to 50GHz frequency range, for various diode sizes, from which a non-linear diode model was derived.

A 180° balanced mixer topology was chosen for this design, using a Lange coupler and an additional 90° line, to provide superior LO-RF isolation performance. Provision was made for biasing the 1x20µm diodes used in the mixer, to allow operation under reduced local oscillator drive levels and to minimise sensitivity to LO power level variations. The chip layout occupies an area of 1.8 x 1.7mm^2 and is shown in figure 4.

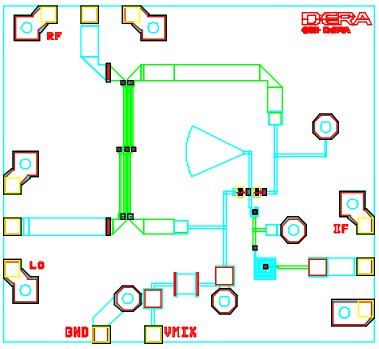

Figure 4 : Mixer layout

* Libra is a trademark of HP-Eesof
** EM is a trademark of Sonnet Software Inc

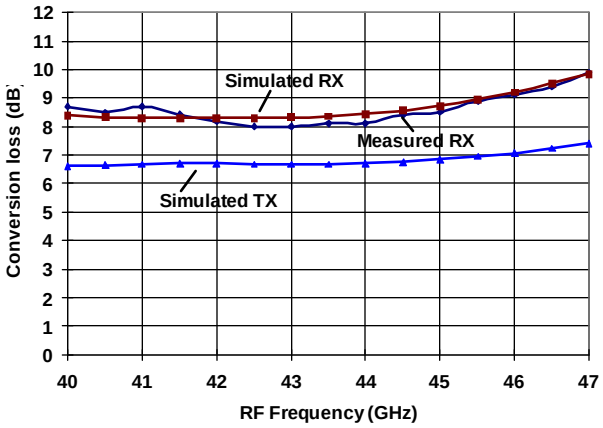

Figure 5 : Measured and simulated conversion loss

A comparison between measured and simulated conversion loss for downconvert operation is shown in figure 5, illustrating excellent agreement. At 44GHz the measured conversion loss was 8dB (LO=37GHz, 8dBm). Conversion loss on upconvert has not yet been measured, however this is predicted to be better than 7dB over the 40 to 46GHz frequency range.

2.3 Doubler-buffer amplifier

The doubler-buffer amplifier was required to provide >13dBm output power at 38GHz, for a fundamental input frequency (19GHz) power level of 0dBm. Both active and passive design approaches were analysed in detail for this design. The favoured approach was to use an active doubler as this offers the potential for conversion gain.

The doubler uses a 4x30µm gate width device biased at pinch-off (Vds=3V, Vgs=-1V) and operates as a half wave rectifier, with matching circuitry used to enhance and extract the second harmonic. Particular care was taken with this design to ensure stability over the whole device IV plane, series resistors were used on the gate for this purpose. In order to boost the output signal level from the doubler and provide a good output match, a 3 stage buffer amplifier was also implemented. Each stage of the buffer amplifier used a 4x60µm device with parallel RLC feedback to reduce sensitivity to process variations. Two open circuit, quarter wavelength, stubs are used on the output of the doubler to provide 30-40dB of fundamental rejection. Figure 6 shows the layout of the combined doubler buffer amplifier. Chip size is 3.2 x 1.47mm^2.

In order to improve the probability of achieving a first pass success for the doubler, both standard EEHEMT non-linear models and physics based non-linear models were used to analyse performance. This type of doubler design is a stringent test of non-linear model accuracy since RF excursions will push the device well into pinch-off and potentially into forward gate conduction. In general it is difficult to obtain closed-form empirical non-linear models that are capable of predicting 2nd and 3rd order harmonic levels with a high degree of accuracy. The use of physics based non-linear models was an attempt to address such issues.

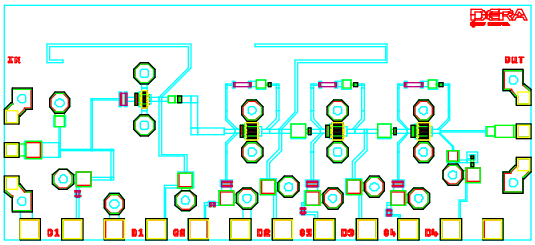

Figure 6 : Layout of doubler-buffer amplifier

Measured results for the doubler-buffer amplifier are shown in figure 7. For an input power level of +1dBm, ≥11dBm output power was obtained over the 32 to 40GHz frequency range. By increasing the input power level to +6dBm, typically 15 to 16dBm of output power was obtained, more than enough to drive the mixer. Fundamental frequency rejection was found to be better than 28dB over the same band.

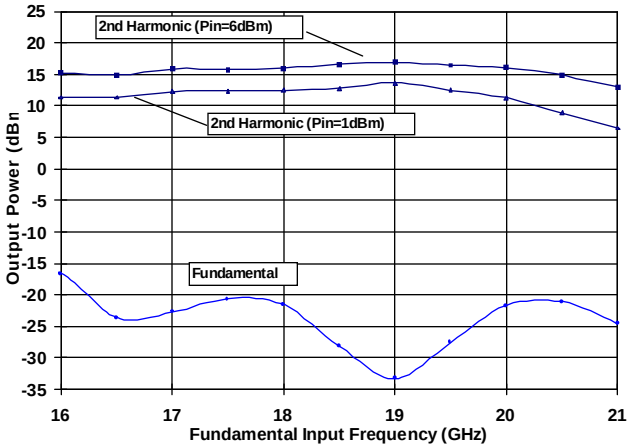

Figure 7 : Measured response of doubler/buffer amplifier

2.4 Low noise block downconvertor

The layout of the complete low noise block downconvertor chip is shown in figure 8 and occupies an area of 3.0 x 3.8mm^2. Minor modifications were made to the design of the individual building block functions in order to achieve flat conversion gain performance. Measured conversion gain was typically 5-8dB depending upon whether the LNA was biased for low noise or high gain. Conversion gain at a fixed LO frequency (19GHz), is shown in figure 9 for low noise bias operation. Noise figure measurements for the complete receiver have not yet been completed, however the predicted noise figure, calculated from measurements on the individual LNA and mixer, is less than 4.5dB at 44GHz as shown in figure 10. The measured RF port and IF port return loss were better than 12dB over the 43.5 to 45.5GHz and 2 to 8GHz frequency bands respectively. Total power dissipation

for this circuit is 400mW (2V, 200mA). A key target for the next design iteration is to reduce this power consumption.

Measurements have been made on two 3" diameter wafers, typical RF functional circuit yields obtained from this first iteration were 70-80%, a high value considering the level of chip complexity.

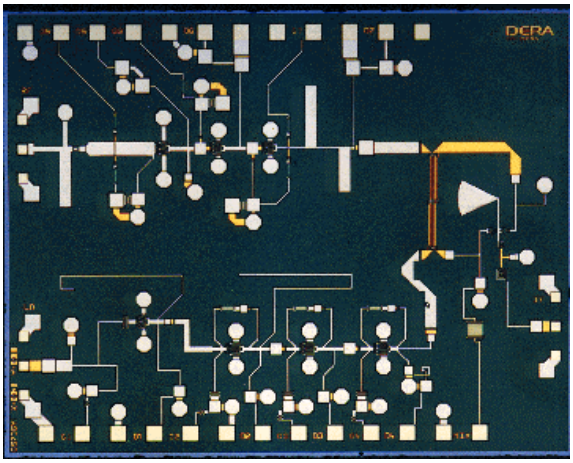

Figure 8 : Photograph of low noise block downconvertor

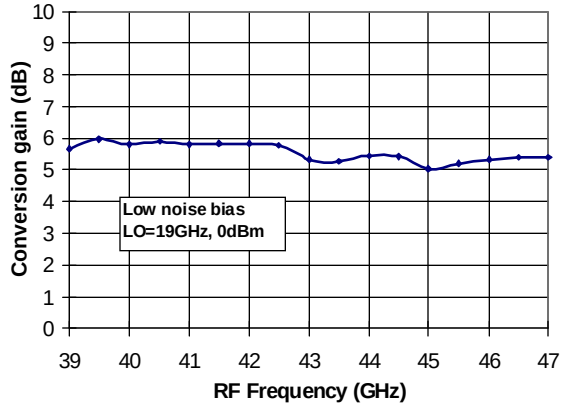

Figure 9 : Measured LNB downconvertor conversion gain

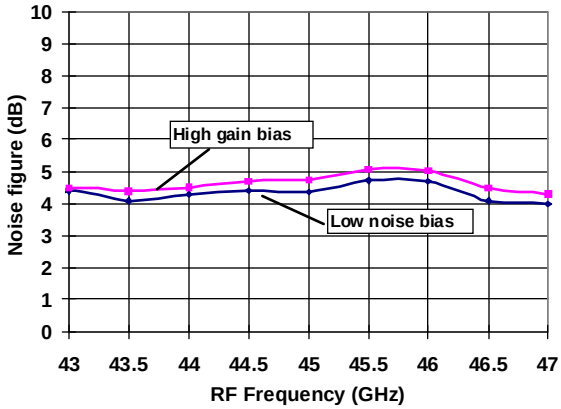

Figure 10 : Predicted LNB downconvertor noise figure

3 Conclusion

A highly integrated MMIC low noise block downconvertor, suitable for use in EHF satellite communication applications, has been fabricated using a commercially available 0.25µm PHEMT GaAs foundry process. Successful results have been obtained for a first iteration, ≤4.5dB noise figure, 5-8dB conversion gain, >12dB port return loss and small chip size (3.0 x 3.8mm^2). These results are important since they show that complex multifunction MMICs can be designed at mm-wave frequencies with high yield and repeatable performance. The use of multifunction MMICs in EHF phased arrays offers a number of key advantages including small size, reduced cost, and improved reliability. These attributes will enable more affordable, novel system architectures to be explored for next generation military satellite communications systems.

4 References

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